This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-28. (Cancelled)

29. (currently amended) A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring a processor interface for an idle condition;

detecting an idle condition in said processor interface before expiration of said timeout task;

in response to said detection, withholding access to a local processor;

~~to identify processor status for determining a time to perform the error recovery instruction for withholding access to a local processor; and~~

performing the error recovery instruction ~~when the monitoring determines a time for performing the error recovery instruction~~ while access to the local processor is withheld; and

forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires.

30. (cancelled)

31. (cancelled)

32. (Currently Amended) The program storage device of claim 29 ~~28,~~ wherein the ~~monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for~~ withholding access to the local processor further comprises:

~~monitoring a processor interface to a host bus for an idle condition;~~

withholding access to the processor interface when the idle condition is detected;

said operations further comprising:

after access to the processor interface is withheld, interrogating ~~all~~ data transfer paths in the processor interface to determine when ~~all~~ the data paths are idle; and

wherein the instruction performing while access to the local processor is withheld includes:

performing the error recovery instruction ~~identifying the time to perform the error recovery instruction~~ when ~~all~~ the data transfer paths are idle.

33. (Previously Presented) The program storage device of claim 32 further comprising resuming normal operations after performing the error recovery instruction.

34. (currently amended) The program storage device of claim 29 ~~28~~ further comprising resuming normal operations after performing the error recovery instruction.

35-40. (cancelled)

41. (Currently amended) An apparatus for use with a local processor and for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic for receiving an error recovery instruction; and

a timer, coupled to the self-quiesce logic, for determining when to force execution of the error recovery instruction;

wherein the self-quiesce logic initiates the timer when the error recovery instruction is received, begins to monitor a processor interface for an idle condition, detects an idle condition in said processor interface before expiration of said timer; in response to said detection, withholds access to a local processor, ~~to identify processor status for determining a time to perform the error recovery instruction for withholding access to a local processor and~~ performs the error recovery instruction ~~when the monitoring determines a time for performing the error recovery instruction~~ while access to the local processor is withheld, and forces performance of the error recovery instruction before an idle condition in said processor interface is detected when the timer expires.

42. (cancelled)

43. (cancelled)

44. (currently amended) The apparatus of claim 41, wherein the self-quiesce logic ~~monitors a processor interface to a host bus to identify processor status for determining a time to perform the error recovery instruction for withholding~~ withholds access to the local processor by ~~monitoring the processor interface for an idle condition,~~ withholding access to the processor interface when the idle condition is detected, after access to the processor interface is withheld, ~~interrogating~~ interrogates ~~all~~ data transfer paths to determine when ~~all~~ the data paths are idle and ~~identifying the time to perform~~ performs the instruction by performing the error recovery instruction when ~~all~~ the data transfer paths are idle.

45. (cancelled)

46. (Previously Presented) The apparatus of claim 41, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

47-52. (cancelled)

53. (currently amended) A method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring a processor interface for an idle condition;

detecting an idle condition in said processor interface before expiration of said timeout task;

in response to said detection, withholding access to a local processor;

~~to identify processor status for determining a time to perform the error recovery instruction for withholding access to a local processor; and~~

performing the error recovery instruction ~~when the monitoring determines a time for performing the error recovery instruction~~ while access to the local processor is withheld; and

forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires.

54-56. (Cancelled)

57. (new) The method of claim 53, wherein the withholding access to a local processor further comprises:

withholding access to the processor interface when the idle condition is detected;

said method further comprising:

after access to the processor interface is withheld, interrogating ~~all~~ data transfer paths in the processor interface to determine when ~~all~~ the data paths are idle; and

wherein the instruction performing while access to the local processor is withheld includes:

performing the error recovery instruction when the data transfer paths are idle.

58. (new) The method of claim 57 further comprising resuming normal operations after performing the error recovery instruction.

59. (new) The method of claim 53 further comprising resuming normal operations after performing the error recovery instruction.

60. (new) An apparatus for determining when to perform an error recovery instruction, comprising:

logic means for receiving an error recovery instruction;

logic means for beginning a timeout task upon receipt of said instruction;

logic means for monitoring a processor interface for an idle condition;

logic means for detecting an idle condition in said processor interface before expiration of said timeout task;

logic means for, in response to said detection, withholding access to a local processor;

logic means for initiating performance of the error recovery instruction while access to the local processor is withheld; and

logic means for forcing initiation of performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires.

61. (new) The apparatus of claim 60, wherein the logic means for withholding access to a local processor includes:

means for withholding access to the processor interface when the idle condition is detected;

said apparatus further comprising:

logic means for, after access to the processor interface is withheld, interrogating ~~all~~ data transfer paths in the processor interface to determine when ~~all~~ the data paths are idle; and

wherein the logic means for initiating instruction performance while access to the local processor is withheld includes:

logic means for initiating performance of the error recovery instruction when the data transfer paths are idle.

62. (new) The apparatus of claim 60 further comprising logic means for resuming normal operations after performing the error recovery instruction.

63. (new) The apparatus of claim 61 further comprising logic means for resuming normal operations after performing the error recovery instruction.